**FlashController Module Description Document**

1. **Introduction**

The SPI Flash controller module (hereinafter referred to as FSHC) has two functions:

* Read instructions from the external SPI Flash for execution;
* Use the external SPI Flash as a common data storage medium for read/write/erase operations.

The external SPI Flash connected to the interface of the FSHC module is mainly used to store programs and serves as the storage space for the programs.

Of course, it can also store data, such as some configuration information of the system, prompt sounds, etc. If a large amount of data information needs to be stored, a Flash medium connected to the SPI module can be used.

The following figure shows the position of FSHC in the chip.

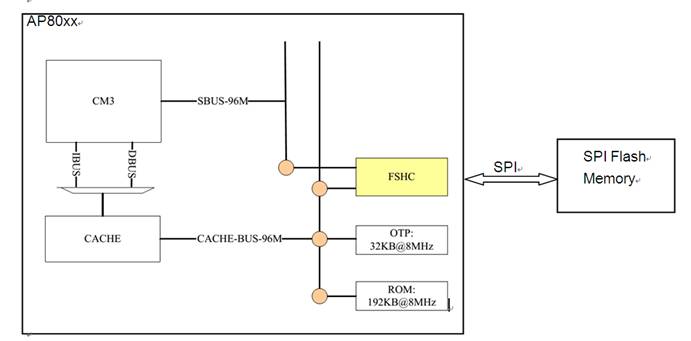


Figure 1 Schematic diagram of the location of FSHC

**2. Instructions for Use**

**2.1 Initialization of the FSHC Module**

FSHC must be initialized before use. Since the program execution requires FSHC to fetch instructions from external Flash, the FSHC initialization code cannot be placed in external Flash. Instead, FSHC initialization is performed in the bootloader of the AP80 series. As a result, user code does not need to concern itself with FSHC initialization.

After the system starts up, the bootloader in OTP is run. Once the bootloader has completed the initialization of FSHC, it can switch to running instructions from Flash. This process is completely transparent to the user.

**2.2 FSHC module interface pins**

The FSHC module has 6 IO pins, as follows:

FSH\_CS, FSH\_SCK, FSH\_SO, FSH\_SI, FSH\_WP and FSH\_HOLD. Among them, FSH\_WP and FSH\_HOLD are two IO devices used in the Quad IO mode (for details, see the relevant Flash documentation). The design requirements for the AP80 series chips stipulate that if the code runs from Flash, the Flash model must support the Quad IO mode. Therefore, if the program runs from Flash, the FSH\_WP and FSH\_HOLD pins must be used.

**2.3 The FSHC Module Provides Two Clock Options**

  fshc\_hpm\_clock: This clock is used in high-performance mode. For Flash devices like the GD model that support HPM mode, this clock can be utilized. The frequency of fshc\_hpm\_clock is fixed at 96MHz;

  fshc\_clock: SPI Flash clock, with four frequency options available:

a) System clock;

b) DPLL 80MHz

c) DPLL 60MHz

d) DPLL 48MHz

fshc\_hpm\_clock is the default configuration during FSHC initialization. It is only applicable to GD Flash. For fshc\_clock, the system clock is used by default during FSHC initialization. If you wish to change or reduce the Flash clock, you can call SpiFlashClkSet in the user code to reconfigure it. For details, refer to the SpiFlashClkSet function description.

**2.4 FSHC Module and Flash Model**

The AP80 series chip design requires that the Flash model support Quad IO mode if the code runs from Flash. Therefore, when selecting a Flash model, ensure that it supports Quad IO mode.

**2.5 Usage Notes for FSHC and LCDC Modules**

From the I/O multiplexing relationship of the AP80 series chips, since the FSHC module and LCDC module share the same pin, if the program is run from Flash, the LCDC module cannot be used simultaneously.

When running the program from SDRAM, the code is copied from the Flash to SDRAM via 1-bit SPI mode from the OTP bootloader, then remapped to SDRAM for execution. The Flash is used solely as a code storage device, allowing the FSH\_WP and FSH\_HOLD pins to be repurposed for other uses, thereby enabling support for the LCDC module.